Rev 1; 9/07

3.3V Spread-Spectrum EconOscillator

DS1086L

General Description

The DS1086L EconOscillator™ is a 3.3V programmable clock generator that produces a spread-spectrum (dithered) square-wave output of frequencies from 130kHz to 66.6MHz. The selectable dithered output reduces radiated-emission peaks by dithering the frequency 0.5%,1%, 2%, 4%, or 8% below the programmed frequency. The DS1086L has a power-down mode and an output-enable control for power-sensitive applications. All the device settings are stored in nonvolatile (NV) EEPROM memory allowing it to operate in stand-alone applications.

Applications

Printers

Copiers

PCs

Computer Peripherals

Cell Phones

Cable Modems

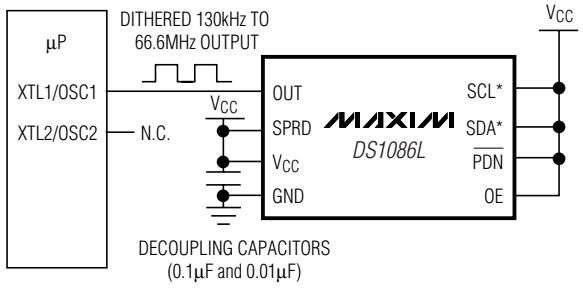
Features

- **User-Programmable Square-Wave Generator**
- **Frequencies Programmable from 130kHz to 66.6MHz**
- **0.5%, 1%, 2%, 4%, or 8% Selectable Dithered Output**
- **Adjustable Dither Rate**
- **Glitchless Output-Enable Control**
- **2-Wire Serial Interface**
- **Nonvolatile Settings**
- **2.7V to 3.6V Supply**
- **No External Timing Components Required**
- **Power-Down Mode**
- **5kHz Master Frequency Step Size**
- **EMI Reduction**
- **Industrial Temperature Range: -40°C to +85°C**

Ordering Information

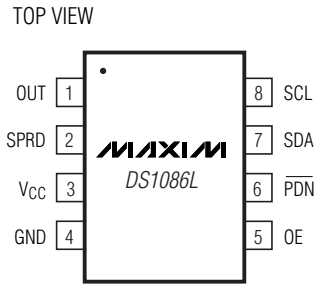
PART	TEMP RANGE	PIN-PACKAGE
DS1086LU	-40°C to +85°C	8 µSOP (118 mil)

Typical Operating Circuit



*SDA AND SCL CAN BE CONNECTED DIRECTLY HIGH IF THE DS1086L NEVER NEEDS TO BE PROGRAMMED IN-CIRCUIT, INCLUDING DURING PRODUCTION TESTING.

Pin Configuration



µSOP

EconOscillator is a trademark of Dallas Semiconductor.

3.3V Spread-Spectrum EconOscillator

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Relative to Ground .....-0.5V to +6.0V
Voltage Range on SPRD, $\overline{PDN}$, OE, SDA, and SCL
Relative to Ground* .....-0.5 to (V_{CC} + 0.5V)

Operating Temperature Range .....-40°C to +85°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A

**This voltage must not exceed 6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7	3.3	3.6	V
High-Level Input Voltage (SDA, SCL, SPRD, $\overline{PDN}$, OE)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL SPRD, $\overline{PDN}$, OE)	V_{IL}		-0.3		0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Output Voltage (OUT)	V_{OH}	I_{OH} = -4mA, V_{CC} = min	2.4			V
Low-Level Output Voltage (OUT)	V_{OL}	I_{OL} = 4mA	0		0.4	V
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	
High-Level Input Current	I_{IH}	V_{CC} = 3.6V			1	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0	-1			µA
Supply Current (Active)	I_{CC}	C_L = 15pF (output at default frequency)			10	mA
Standby Current (Power-Down)	I_{CCQ}	Power-down mode			10	µA

MASTER OSCILLATOR CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Master Oscillator Frequency	f_{OSC}	(Note 2)		33.3		66.6	MHz
Default Master Oscillator Frequency	f_0	Factory-programmed default			48.65		MHz
Master Oscillator Frequency Tolerance	$\frac{\Delta f_0}{f_0}$	V_{CC} = 3.3V, T_A = +25°C (Notes 3,17)	Default frequency(f_0)	-0.5		+0.5	%
			DAC step size	-0.5		+0.5	
Voltage Frequency Variation	$\frac{\Delta f_V}{f_0}$	Over voltage range, T_A = +25°C (Note 4)	Default frequency	-0.75		+0.75	%
			DAC step size	-0.75		+0.75	
Temperature Frequency Variation	$\frac{\Delta f_T}{f_0}$	Over temperature range, V_{CC} = 3.3V (Note 5)	Default frequency	-2.0		+0.75	%
			66.6MHz	-2.0		+0.75	
			33.3MHz	-2.5		+0.75	
Dither Frequency Range (Note 6)	$\frac{\Delta f}{f_0}$	Prescaler bits JS2, JS1, JS0 = 000			0.5		%
		Prescaler bits JS2, JS1, JS0 = 001			1		
		Prescaler bits JS2, JS1, JS0 = 010			2		
		Prescaler bits JS2, JS1, JS0 = 100			4		
		Prescaler bits JS2, JS1, JS0 = 111			8		
Integral Nonlinearity of Frequency	INL	Entire range (Note 7)		-0.6		+0.3	%
DAC Step Size		Δ between two consecutive DAC values (Note 8)			5		kHz
DAC Span		Frequency range for one offset setting (Table 2)			5.12		MHz
DAC Default		Factory default register setting			500		decimal
Offset Step Size		Δ between two consecutive offset values (Table 2)			2.56		MHz
Offset Default	OS	Factory default OFFSET register setting (5 LSBs) (Table 2)			RANGE (5 LSBs of RANGE register)		hex
Dither Rate		Prescaler bits JS4, JS3 = 00			f_0/8192		Hz
		Prescaler bits JS4, JS3 = 01			f_0/4096		
		Prescaler bits JS4, JS3 = 10			f_0/2048		

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Stable After Prescaler Change					1	period
Frequency Stable After DAC or Offset Change	$t_{DACstab}$	(Note 9)		0.1	1	ms
Power-Up Time	$t_{por} + t_{stab}$	(Note 10)		0.1	0.5	ms
Enable of OUT After Exiting Power-Down Mode	t_{stab}	(Note 18)			200	µs
OUT High-Z After Entering Power-Down Mode	t_{pdn}				100	µs
Load Capacitance	C_L	(Note 11)		15	50	pF
Output Duty Cycle (OUT)		Default frequency	45		55	%
Rise and Fall Time (OE, $\overline{PDN}$)					1	µs

AC ELECTRICAL CHARACTERISTICS—2-WIRE INTERFACE

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	(Note 12)			400	kHz
		Standard mode				100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	(Note 12)	1.3			µs
		Standard mode		4.7			
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast mode	(Notes 12, 13)	0.6			µs
		Standard mode		4.0			
LOW Period of SCL	t_{LOW}	Fast mode	(Note 12)	1.3			µs
		Standard mode		4.7			
HIGH Period of SCL	t_{HIGH}	Fast mode	(Note 12)	0.6			µs
		Standard mode		4.0			
Setup Time for a Repeated START	$t_{SU:STA}$	Fast mode	(Note 12)	0.6			µs
		Standard mode		4.7			
Data Hold Time	$t_{HD:DAT}$	Fast mode	(Notes 12, 14, 15)	0		0.9	µs
		Standard mode					
Data Setup Time	$t_{SU:DAT}$	Fast mode	(Note 12)	100			ns
		Standard mode		250			
Rise Time of Both SDA and SCL Signals	t_R	Fast mode	(Note 16)	$20 + 0.1C_B$		300	ns
		Standard mode		$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals	t_F	Fast mode	(Note 16)	$20 + 0.1C_B$		300	ns
		Standard mode		$20 + 0.1C_B$		1000	

AC ELECTRICAL CHARACTERISTICS—2-WIRE INTERFACE (continued)

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for STOP	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 16)			400	pF
EEPROM Write Cycle Time	t_{WR}				10	ms
Input Capacitance	C_I			5		pF

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Writes		+70°C	10,000			

Note 1: All voltages are referenced to ground.

Note 2: DAC and OFFSET register settings must be configured to maintain the master oscillator frequency within this range. Correct operation of the device is not guaranteed if these limits are exceeded.

Note 3: This is the absolute accuracy of the master oscillator frequency at the default settings.

Note 4: This is the change that is observed in master oscillator frequency with changes in voltage from nominal voltage at T_A = +25°C.

Note 5: This is the percentage frequency change from the +25°C frequency due to temperature at V_{CC} = 3.3V. The maximum temperature change varies with the master oscillator frequency setting. The minimum occurs at the default master oscillator frequency ($f_{default}$). The maximum occurs at the extremes of the master oscillator frequency range (33.3MHz or 66.6MHz).

Note 6: The dither deviation of the master oscillator frequency is unidirectional and lower than the undithered frequency.

Note 7: The integral nonlinearity of the frequency is a measure of the deviation from a straight line drawn between the two endpoints ($f_{osc(MIN)}$ to $f_{osc(MAX)}$) of the range. The error is in percentage of the span.

Note 8: This is true when the prescaler = 1.

Note 9: Frequency settles faster for small changes in value. During a change, the frequency transitions smoothly from the original value to the new value.

Note 10: This indicates the time elapsed between power-up and the output becoming active. An on-chip delay is intentionally introduced to allow the oscillator to stabilize. t_{stab} is equivalent to approximately 512 master clock cycles and therefore depends on the programmed clock frequency.

Note 11: Output voltage swings can be impaired at high frequencies combined with high output loading.

Note 12: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line at least $t_{R\ MAX}$ + $t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.

Note 13: After this period, the first clock pulse is generated.

Note 14: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to as the $V_{IH\ MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 15: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 16: C_B—total capacitance of one bus line, timing referenced to 0.9 x V_{CC} and 0.1 x V_{CC}.

Note 17: Typical frequency shift due to aging is ±0.5%. Aging stressing includes Level 1 moisture reflow preconditioning (24hr +125°C bake, 168hr 85°C/85%RH moisture soak, and three solder reflow passes +240 +0/-5°C peak) followed by 1000hr max V_{CC} biased 125°C HTOL, 1000 temperature cycles at -55°C to +125°C, 96hr 130°C/85%RH/3.6V HAST and 168hr 121°C/2 ATM Steam/Unbiased Autoclave.

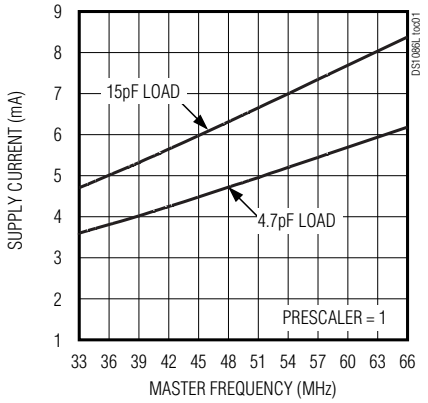
Note 18: t_{stab} is the time required after exiting power-down to the beginning of output oscillations. In addition, a delay of $t_{DACstab}$ is required before the frequency will be within its specified tolerance.

3.3V Spread-Spectrum EconOscillator

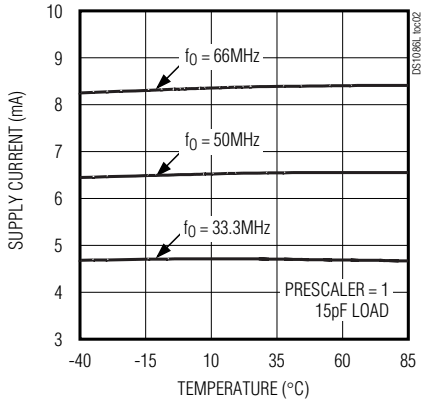
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.)

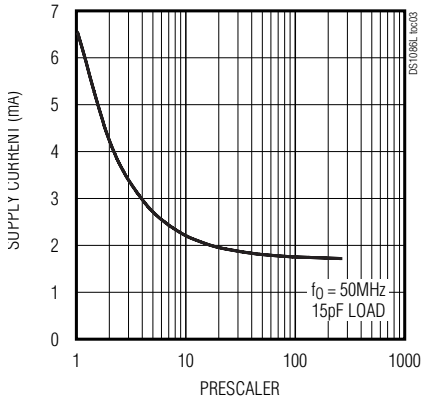
SUPPLY CURRENT vs. MASTER OSCILLATOR FREQUENCY



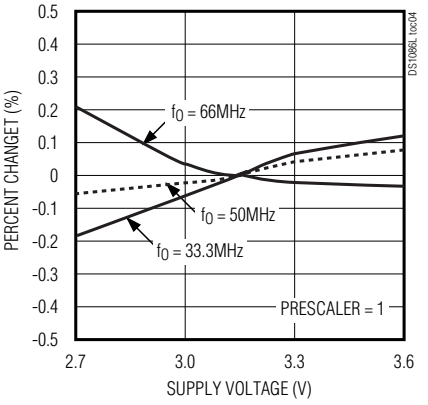
SUPPLY CURRENT vs. TEMPERATURE



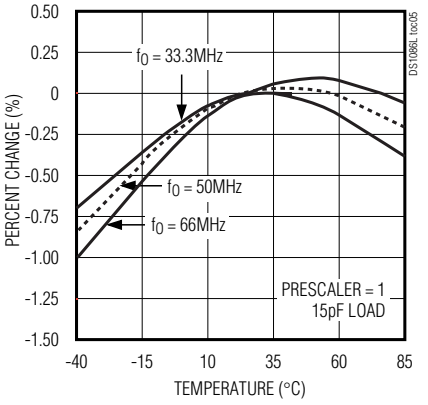
SUPPLY CURRENT vs. PRESCALER



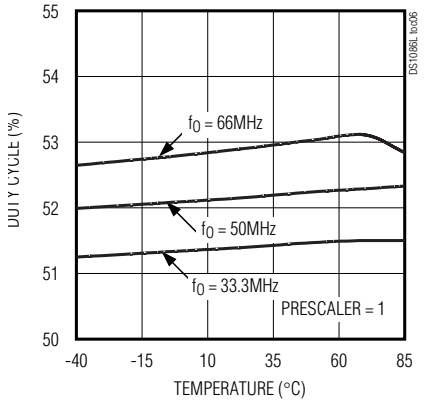
MASTER OSCILLATOR FREQUENCY PERCENT CHANGE vs. SUPPLY VOLTAGE



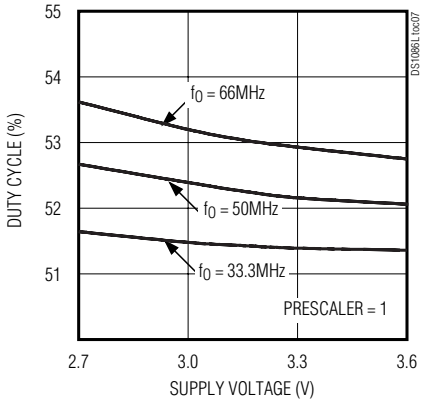
MASTER OSCILLATOR FREQUENCY PERCENT CHANGE vs. TEMPERATURE



DUTY CYCLE vs. TEMPERATURE



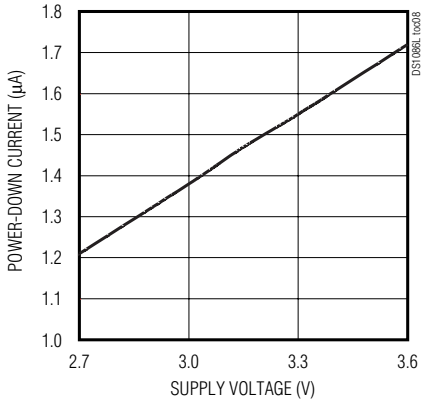
DUTY CYCLE vs. SUPPLY VOLTAGE



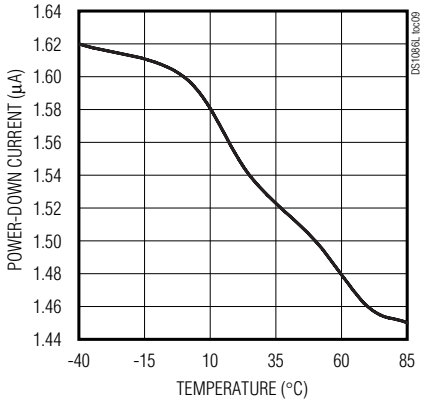
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.)

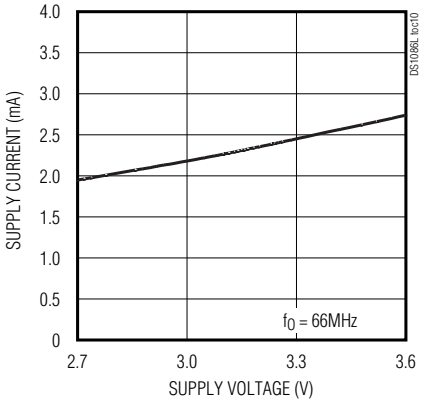
POWER-DOWN CURRENT vs. SUPPLY VOLTAGE



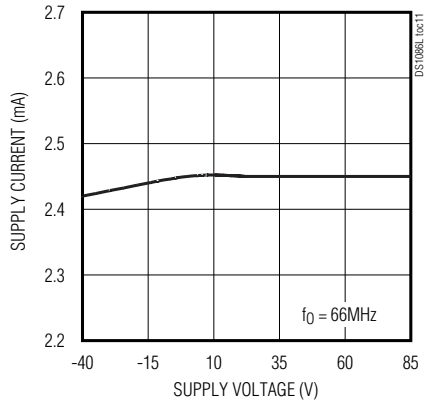
POWER-DOWN CURRENT vs. TEMPERATURE



SUPPLY CURRENT WITH OUTPUT DISABLED vs. SUPPLY VOLTAGE



SUPPLY CURRENT WITH OUTPUT DISABLED vs. TEMPERATURE



3.3V Spread-Spectrum EconOscillator

Pin Description

PIN	NAME	FUNCTION
1	OUT	Oscillator Output. The output frequency is determined by the OFFSET, DAC, and prescaler registers.
2	SPRD	Dither Enable. When the pin is high, the dither is enabled. When the pin is low, the dither is disabled.
3	V_{CC}	Power Supply
4	GND	Ground
5	OE	Output Enable. When the pin is high, the output buffer is enabled. When the pin is low, the output is disabled but the master oscillator is still on.
6	$\overline{PDN}$	Power-Down. When the pin is high, the master oscillator is enabled. When the pin is low, the master oscillator is disabled (power-down mode).
7	SDA	2-Wire Serial Data. This pin is for serial data transfer to and from the device. The pin is open drain and can be wire-ORed with other open-drain or open-collector interfaces.
8	SCL	2-Wire Serial Clock. This pin is used to clock data into the device on rising edges and clock data out on falling edges.

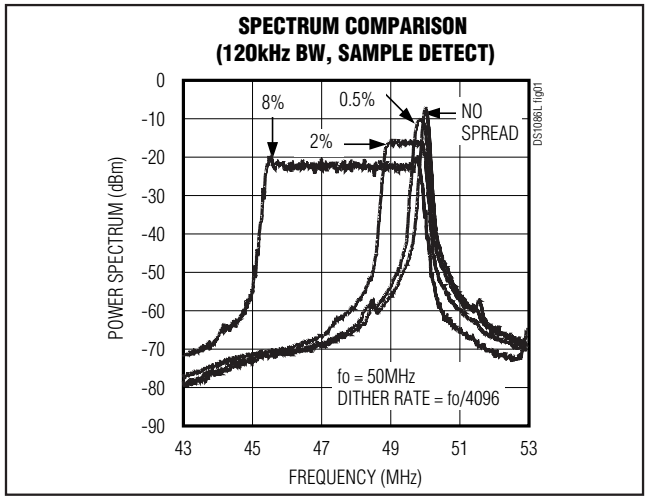


Figure 1. Clock Spectrum Dither Comparison

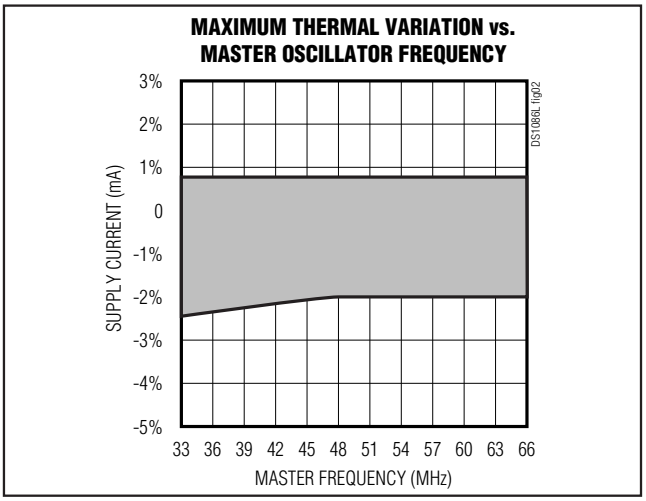
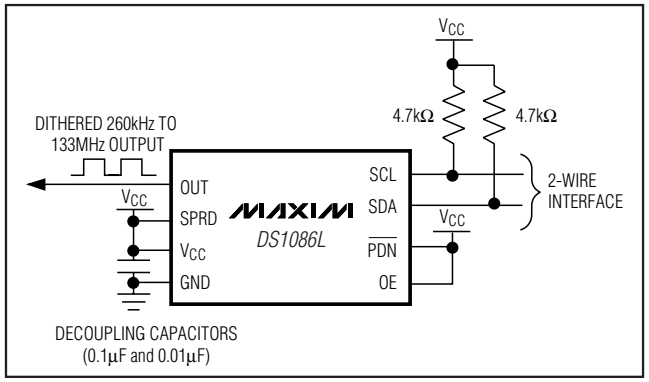
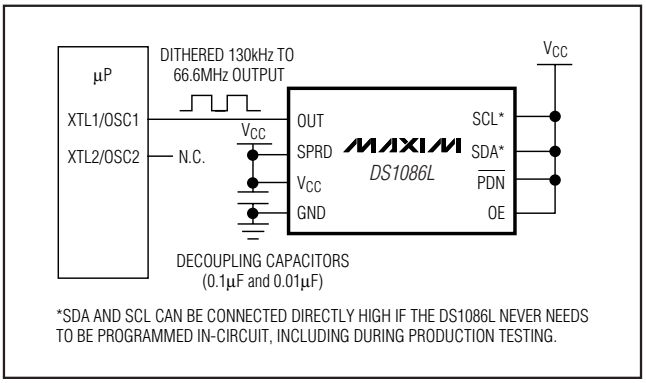


Figure 2. Temperature Variation Over Frequency

Processor-Controlled Mode



Stand-Alone Mode



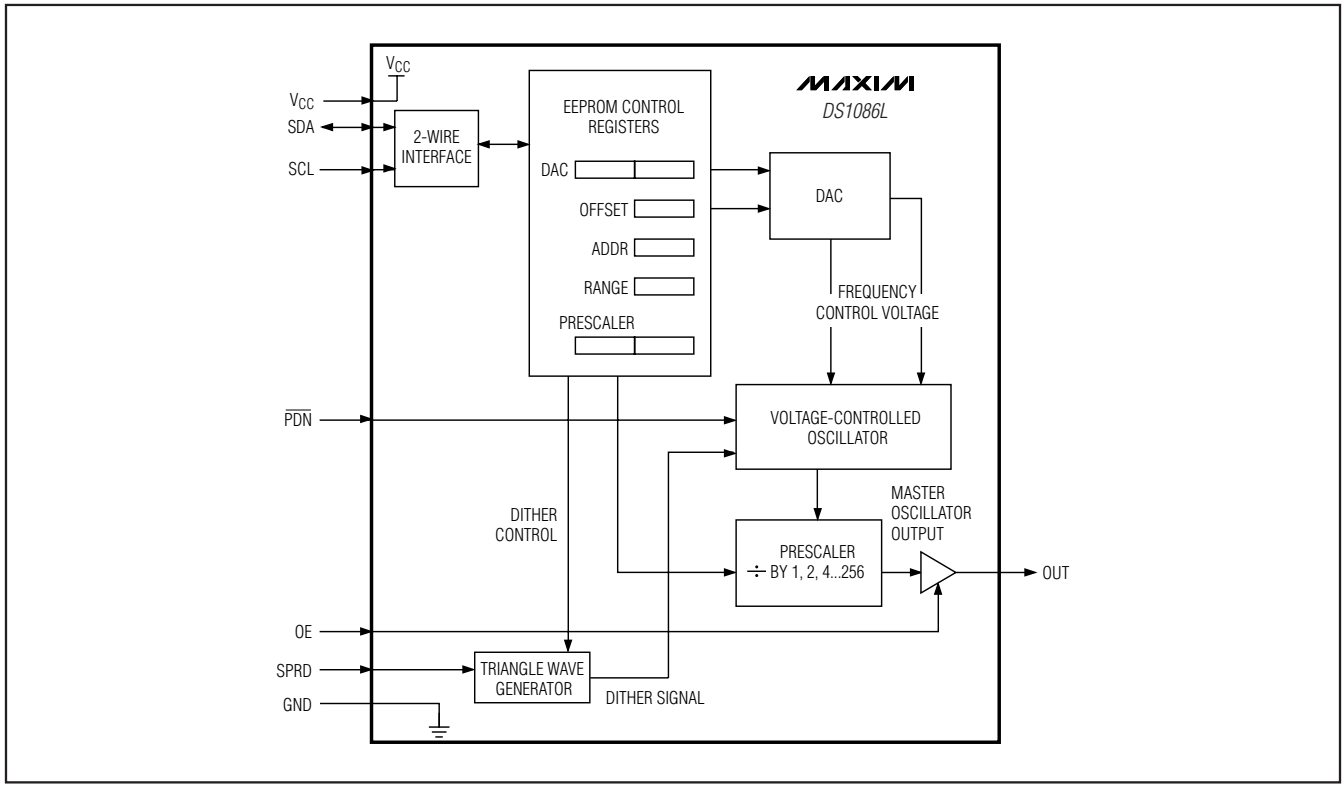


Figure 3. Block Diagram

Detailed Description

A block diagram of the DS1086L is shown in Figure 3. The internal master oscillator generates a square wave with a 33.3MHz to 66.6MHz frequency range. The frequency of the master oscillator can be programmed with the DAC register over a two-to-one range in 5kHz steps. The master oscillator range is larger than the range possible with the DAC step size, so the OFFSET register is used to select a smaller range of frequencies over which the DAC spans. The prescaler can then be set to divide the master oscillator frequency by 2^x (where x equals 0 to 8) before routing the signal to the output (OUT) pin.

A programmable triangle-wave generator injects an offset element into the master oscillator to dither its output 0.5%, 1%, 2%, 4%, or 8%. The dither magnitude is controlled by the JS2, JS1, and JS0 bits in the PRESCALER word and enabled with the SPRD pin. Futhermore, the dither rate is controlled by the JS4 and JS3 bits in the PRESCALER word and determines the frequency of the dither. The maximum spectral attenuation occurs when the prescaler is set to 1 and is reduced by 2.7dB for every factor of 2 that is used in the prescaler. This happens because the prescaler's divider function tends to average the dither in creating the lower frequency. However, the most stringent spectral emission limits are imposed on the higher frequencies where the prescaler is set to a low divider ratio.

The external control input, OE, gates the clock output buffer. The $\overline{PDN}$ pin disables the master oscillator and turns off the clock output for power-sensitive applications*. On power-up, the clock output is disabled until power is stable and the master oscillator has generated 512 clock cycles. Both controls feature a synchronous enable that ensures there are no output glitches when the output is enabled.

The control registers are programmed through a 2-wire interface and are used to determine the output frequency and settings. Once programmed into EEPROM, since the register settings are NV, the settings only need to be reprogrammed if it is desired to reconfigure the device.

**The power-down command must persist for at least two output frequency cycles plus 10µs for deglitching purposes.*

3.3V Spread-Spectrum EconOscillator

Table 1. Register Summary

REGISTER	ADDR	MSB			BINARY				LSB	FACTORY DEFAULT	ACCESS
PRESCALER	02h	JS4	JS3	JS2	JS1	JS0	LO/$\overline{HiZ}$	P3	P2	01100000	R/W
PRESCALER	—	P1	P0	X_X	X_X	X_X	X_X	X_X	X_X	00XXXXX	R/W
DAC (MSB)	08h	b9	b8	b7	b6	b5	b4	b3	b2	01111101b	R/W
DAC (LSB)	—	b1	b0	X_0	X_0	X_0	X_0	X_0	X_0	00000000b	R/W
OFFSET	0Eh	X_1	X_1	X_1	b4	b3	b2	b1	b0	111-----b	R/W
ADDR	0Dh	X_1	X_1	X_1	X_1	WC	A2	A1	A0	11110000b	R/W
RANGE	37h	X_X	X_X	X_X	b4	b3	b2	b1	b0	xxx-----b	R
WRITE EE	3Fh	NO DATA								—	—

X_0 = Don't care, reads as zero.

X_1 = Don't care, reads as one.

X_X = Don't care, reads indeterminate.

X = Don't care.

Table 2. Offset Settings

OFFSET	FREQUENCY RANGE (MHz)
OS - 6	30.74 to 35.86
OS - 5	33.30 to 38.42
OS - 4	35.86 to 40.98
OS - 3	38.42 to 43.54
OS - 2	40.98 to 46.10
OS - 1	43.54 to 48.66
OS*	46.10 to 51.22
OS + 1	48.66 to 53.78
OS + 2	51.22 to 56.34
OS + 3	53.78 to 58.90
OS + 4	56.34 to 61.46
OS + 5	58.90 to 64.02
OS + 6	61.46 to 66.58

**Factory default setting. OS is the integer value of the five LSBs of the RANGE register.*

The output frequency is determined by the following equation:

$$f_{OUTPUT} = \frac{(\text{MIN FREQUENCY OF SELECTED OFFSET RANGE}) + (\text{DAC VALUE} \times 5\text{kHz STEP SIZE})}{\text{PRESCALER}}$$

where: *min frequency of selected OFFSET range* is the lowest frequency (shown in Table 2 for the corresponding offset).

DAC value is the value of the DAC register (0 to 1023).

Prescaler is the value of 2^x where x = 0 to 8.

See the *Example Frequency Calculations* section for a more in-depth look at using the registers.

Register Definitions

The DS1086L registers are used to program the output frequency, dither percent, dither rate, and 2-wire address. Table 1 shows a summary of the registers and detailed descriptions follow below.

PRESCALER (02h)

The PRESCALER word is a two-byte value containing control bits for the prescaler (P3 to P0), output control (Lo/$\overline{HiZ}$), the jitter rate (JS4 to JS3), as well as control bits for the jitter percentage (JS2 to JS0). The PRESCALER word is read and written using two-byte reads and writes beginning at address 02h.

JS4 to JS3: Jitter Rate. This is the frequency of the triangle wave generator and the modulation frequency that the output is dithered. It can be programmed to the master oscillator frequency, f_{OSC}, divided by either 8192, 4096, or 2048.

JS4	JS3	JITTER RATE
0	0	f_{OSC}/8192
0	1	f_{OSC}/4096 (default)
1	0	f_{OSC}/2048

JS2 to JS0: Jitter Percentage. These three bits select the amount of jitter in percent. The SPRD pin must be a logic high for the jitter to be enabled. Bit combinations not shown are reserved.

JS2	JS1	JS0	JITTER %
0	0	0	0.5
0	0	1	1
0	1	0	2
1	0	0	4
1	1	1	8

Lo/$\overline{\text{HiZ}}$: Output Low or High-Z. This bit determines the state of the output pin when the device is in power-down mode or when the output is disabled. If Lo/$\overline{\text{HiZ}}$ = 0, the output is $\overline{\text{HiZ}}$ when in power-down or disabled. If Lo/$\overline{\text{HiZ}}$ = 1, the output is held low when in power-down or disabled.

P3 to P0: Prescaler Divider. These bits divide the master oscillator frequency by 2^X, where x is P3 to P0 and can be from 0 to 8. Any prescaler value entered greater than 8 decodes as 8.

DAC (08h)

B9 to B0: DAC Setting. The DAC word sets the master oscillator frequency to a specific value within the current offset range. Each step of the DAC changes the master oscillator frequency by 5kHz. The DAC word is read and written using two-byte reads and writes beginning at address 08h.

OFFSET (0Eh)

B4 to B0: Offset. This value selects the master oscillator frequency range that can be generated by varying the DAC word. Valid frequency ranges are shown in Table 2. Correct operation of the device is not guaranteed for values of OFFSET not shown in the table.

The default offset value (OS) is factory trimmed and can vary from device to device. Therefore, to change frequency range, OS must be read so the new offset value can be calculated relative to the default. For example, to generate a master oscillator frequency within the largest range (61.4MHz to 66.6MHz), Table 2 indicates that the OFFSET must be programmed to OS + 6. This is done by reading the RANGE register and adding 6 to the value of bits B4 to B0. The result is then written into bits B4 to B0 of the OFFSET register. Additional examples are provided in the *Example Frequency Calculations* section.

RANGE (37h)

B4 to B0: Range: This read-only, factory programmed value is a copy of the factory default offset (OS). OS is required to program new master oscillator frequencies shown in Table 2. The read-only backup is important because the offset register is EEPROM and is likely to be overwritten.

ADDR (0Dh)

WC: EEPROM Write Control Bit. The WC bit enables/disables the automatic writing of registers to EEPROM. This prevents EEPROM wear out and eliminates the EEPROM write cycle time. If WC = 0 (default), register writes are automatically written to EEPROM. If WC = 1, register writes are stored in SRAM and only written into EEPROM when the user sends a WRITE EE command. If power is cycled to the device, then the last value stored in EEPROM is recalled. WC = 1 is ideal for applications that frequently modify the frequency/registers.

Regardless of the value of the WC bit, the value of the ADDR register is always written immediately to EEPROM.

A2 to A0: Device Address Bits. These bits determine the 2-wire slave address of the device. They allow up to eight devices to be attached to the same 2-wire bus and to be addressed individually.

WRITE EE Command (3Fh)

This command can be used when WC = 1 (see the WC bit in ADDR register) to transfer all registers from SRAM into EEPROM. The time required to store the values is one EEPROM write cycle time. This command is not needed if WC = 0.

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Example Frequency Calculations

Example #1: ***Calculate the register values needed to generate a desired output frequency of 11.0592MHz.***

Since the desired frequency is not within the valid master oscillator range of 33.3MHz to 66.6MHz, the prescaler must be used. Valid prescaler values are 2^X where x equals 0 to 8 (and x is the value that is programmed into the P3 to P0 bits of the PRESCALER register). Equation 1 shows the relationship between the desired frequency, the master oscillator frequency, and the prescaler.

$$f_{DESIRED} = \frac{f_{MASTER\ OSCILLATOR}}{prescaler} = \frac{f_{MASTER\ OSCILLATOR}}{2^X} \quad (1)$$

By trial and error, x is incremented from 0 to 8 in Equation 2, finding values of x that yield master oscillator frequencies within the range of 33.3MHz to 66.6MHz.

Equation 2 shows that a prescaler of 4 (x = 2) and a master oscillator frequency of 44.2368MHz generates our desired frequency. Writing 0080h to the PRESCALER register sets the PRESCALER to 4. Be aware that other settings also reside in the PRESCALER register.

$$f_{MASTER\ OSCILLATOR} = f_{DESIRED} \times prescaler = f_{DESIRED} \times 2^X$$
$$f_{MASTER\ OSCILLATOR} = 11.0592MHz \times 2^2 = 44.2368MHz \quad (2)$$

Once the target master oscillator frequency has been calculated, the value of offset can be determined. Using Table 2, 44.2368MHz falls within both OS - 1 and OS - 2. However, choosing OS - 1 would be a poor choice since 44.2368MHz is so close to OS - 1's minimum frequency. On the other hand, OS - 2 is ideal since 44.2368MHz is close to the center of OS - 2's frequency span. Before the OFFSET register can be programmed, the default value of offset (OS) must be read from the RANGE register (last five bits). In this example, 12h (18 decimal) was read from the RANGE register. OS - 2 for this case is 10h (16 decimal). This is the value that is written to the OFFSET register.

Finally, the two-byte DAC value needs to be determined. Since OS - 2 only sets the range of frequencies, the DAC selects one frequency within that range as shown in Equation 3.

$$f_{MASTER\ OSCILLATOR} = (MIN\ FREQUENCY\ OF\ SELECTED\ OFFSET\ RANGE) + (DAC\ value \times 5kHz) \quad (3)$$

Valid values of DAC are 0 to 1023 (decimal) and 5kHz is the step size. Equation 4 is derived from rearranging Equation 3 and solving for the DAC value.

$$DAC\ VALUE = \frac{(f_{MASTER\ OSCILLATOR} - MIN\ FREQUENCY\ OF\ SELECTED\ OFFSET\ RANGE)}{5kHz\ STEP\ SIZE} \quad (4)$$

$$DAC\ VALUE = \frac{(44.2368MHz - 41.0MHz)}{5kHz\ STEP\ SIZE}$$
$$= 647.36 \approx 647\ (decimal)$$

Since the two-byte DAC register is left justified, 647 is converted to hex (0287h) and bit-wise shifted left six places. The value to be programmed into the DAC register is A1C0h.

In summary, the DS1086L is programmed as follows:

PRESCALER = 0080h

OFFSET = OS - 2 or 10h (if range was read as 12h)

DAC = A1C0h

Notice that the DAC value was rounded. Unfortunately, this means that some error is introduced. To calculate how much error, a combination of Equation 1 and Equation 3 is used to calculate the expected output frequency. See Equation 5.

$$f_{OUTPUT} = \frac{(MIN\ FREQUENCY\ OF\ SELECTED\ OFFSET\ RANGE) + (DAC\ VALUE \times 5kHz\ STEP\ SIZE)}{prescaler} \quad (5)$$

$$f_{OUTPUT} = \frac{(41.0MHz) + (647 \times 5kHz)}{4} = \frac{44.235MHz}{4} = 11.05875MHz$$

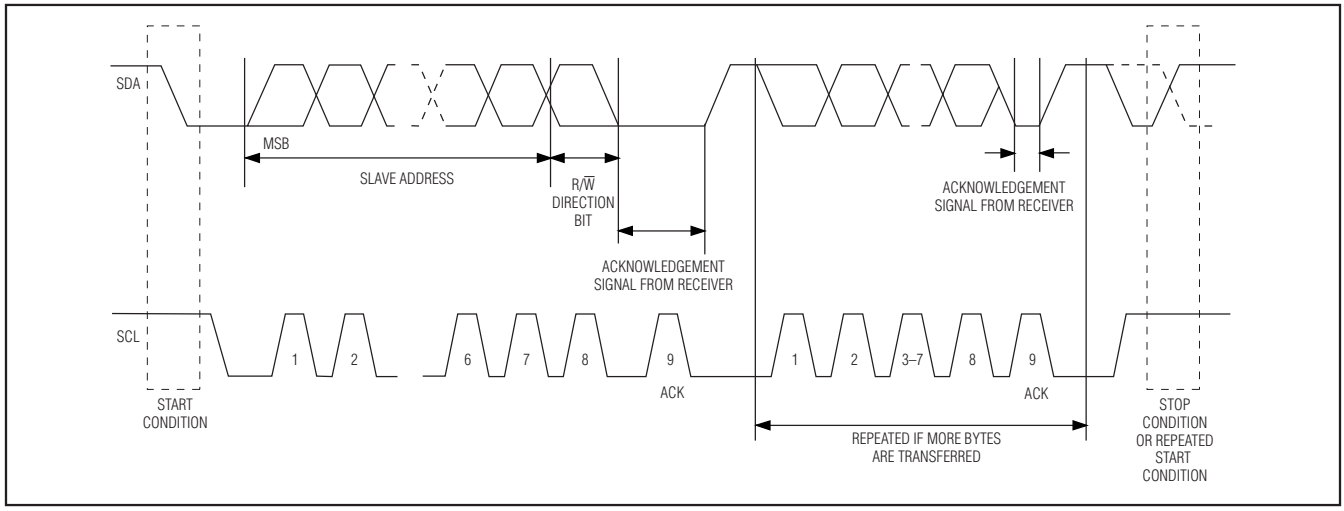

Figure 4. 2-Wire Data Transfer Protocol

The expected output frequency is not exactly equal to the desired frequency of 11.0592MHz. The difference is 450Hz. In terms of percentage, Equation 6 shows that the expected error is 0.004%. The expected error assumes typical values and does not include deviations from the typical as specified in the electrical tables.

$$\%ERROR_{EXPECTED} = \frac{f_{DESIRED} - f_{EXPECTED}}{f_{DESIRED}} \times 100 \quad (6)$$

$$\%ERROR_{EXPECTED} = \frac{11.0592MHz - 11.05875MHz}{11.0592MHz} \times 100 = \frac{450Hz}{11.0592MHz} \times 100 = 0.004\%$$

Example #2: *Calculate the register values needed to generate a desired output frequency of 50MHz.*

Since the desired frequency is already within the valid master oscillator frequency range, the prescaler is set to divide by 1, and hence, PRESCALER = 0000h (currently ignoring the other setting). (7)

$$f_{MASTER\ OSCILLATOR} = 50.0MHz \times 2^0 = 50.0MHz$$

Next, looking at Table 2, OS + 1 provides a range of frequencies centered around the desired frequency. To determine what value to write to the OFFSET register, the RANGE register must first be read. Assuming 12h was read in this example, 13h (OS + 1) is written to the OFFSET register.

Finally, the DAC value is calculated as shown in Equation 8. (8)

$$DAC\ VALUE = \frac{(50.0MHz - 48.6MHz)}{5kHz\ STEP\ SIZE} = 280.00\ (decimal)$$

The result is then converted to hex (0118h) and then left-shifted, resulting in 4600h to be programmed into the DAC register.

In summary, the DS1086L is programmed as follows:

PRESCALER = 0000h

OFFSET = OS + 1 or 13h (if RANGE was read as 12h)

DAC = 4600h

$$f_{OUTPUT} = \frac{(48.6MHz) + (280 \times 5kHz)}{2^0} = \frac{50.0MHz}{1} = 50.0MHz \quad (9)$$

Since the expected output frequency is equal to the desired frequency, the calculated error is 0%.

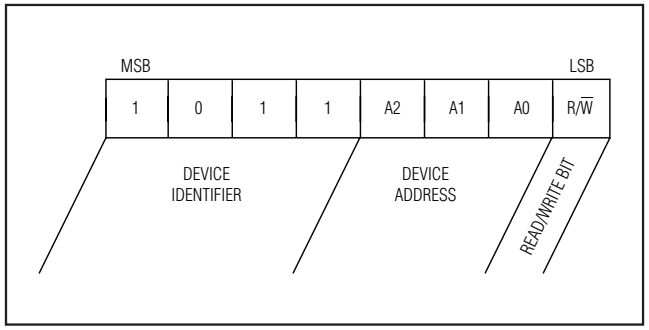

Figure 5. Slave Address

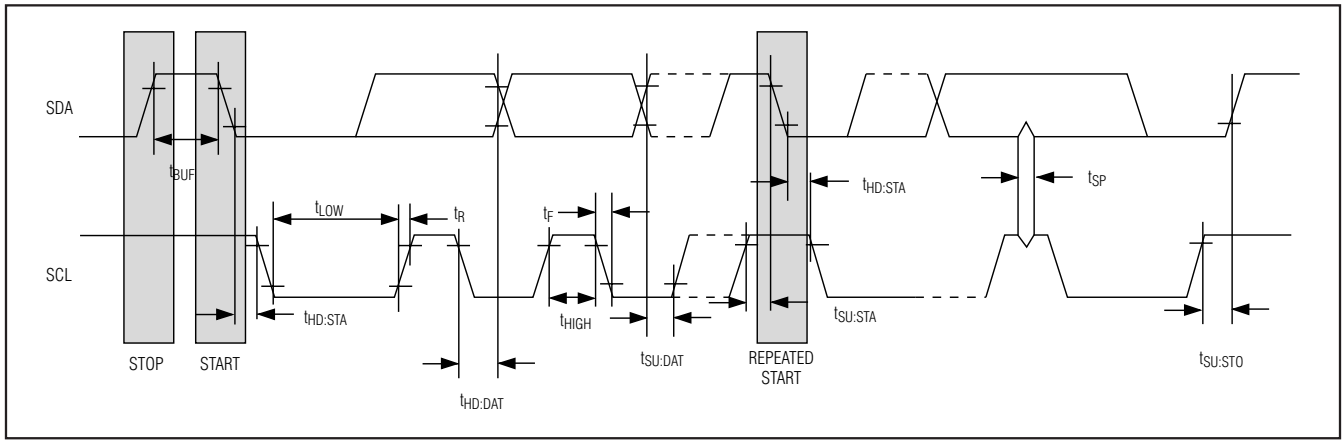

Figure 6. 2-Wire AC Characteristics

2-Wire Serial Port Operation

2-Wire Serial Data Bus

The DS1086L communicates through a 2-wire serial interface. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1086L operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figures 4 and 6):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP con-

ditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1086L works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. When the DS1086L EEPROM is being written to, it is not able to perform additional responses. In this case, the slave DS1086L sends a not acknowledge to any data transfer request made by the master. It resumes normal operation when the EEPROM operation is complete.

A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figures 4, 5, 6, and 7 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2) Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1086L can operate in the following two modes:

Slave receiver mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1086L while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Address

Figure 5 shows the first byte sent to the device. It includes the device identifier, device address, and the R/$\overline{W}$ bit. The device address is determined by the ADDR register.

Registers/Commands

See Table 1 for the complete list of registers/commands and Figure 7 for an example of using them.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS1086L, decouple the power supply with 0.01µF and 0.1µF high-quality, ceramic, surface-mount capacitors. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. These capacitors should be placed as close to pins 3 and 4 as possible.

Stand-Alone Mode

SCL and SDA cannot be left floating when they are not used. If the DS1086L never needs to be programmed in-circuit, including during production testing, SDA and SCL can be tied high. The SPRD pin must be tied either high or low.

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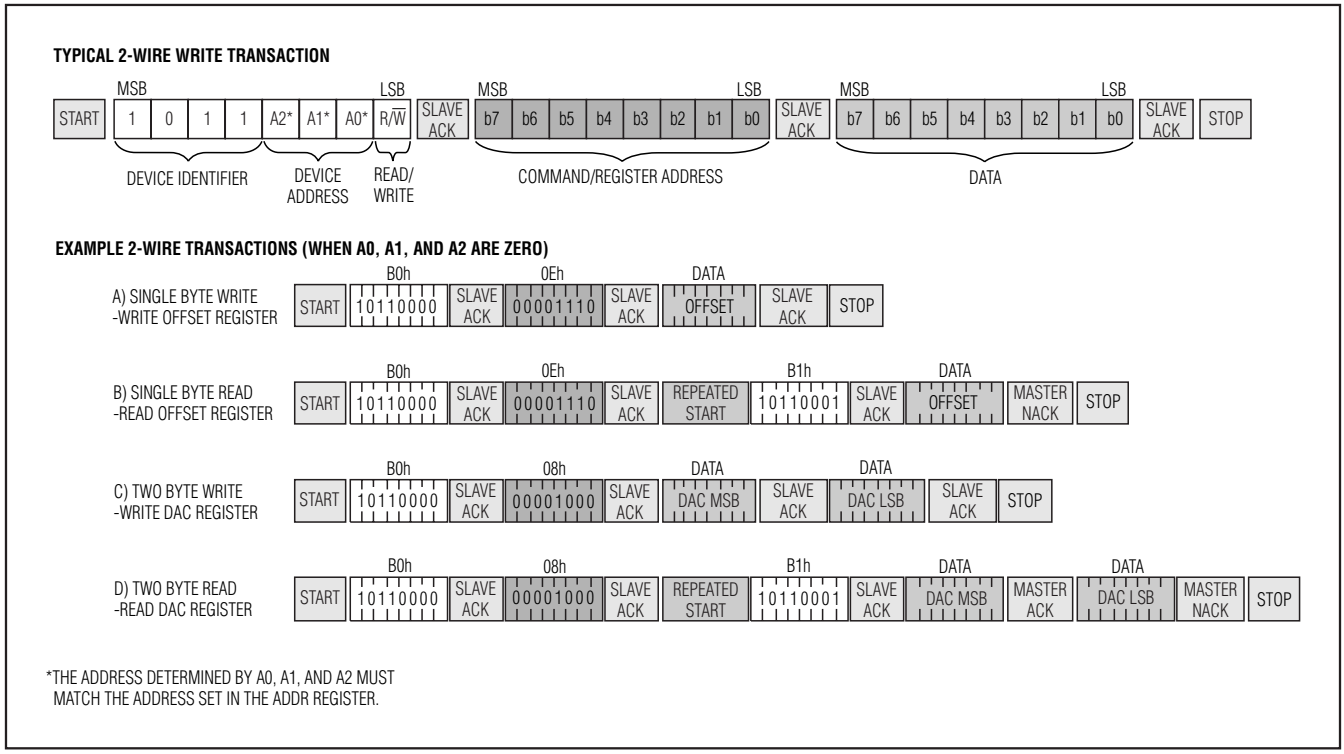

Figure 7. 2-Wire Transactions

Chip Topology

TRANSISTOR COUNT: 9052

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

Revision History

Pages changed at Rev 1: 10